365 233

5841731

FIG. 1A CLK

FIG. 1B COMMAND

FIG. 1C ADDRESS

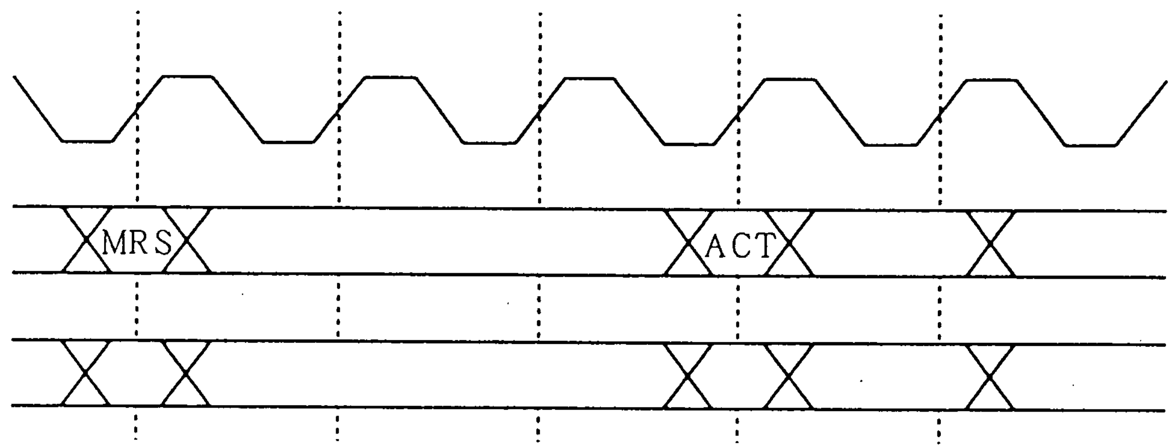


FIG. 1D

A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A0
"L"	"L"	"L"	"L"	"L"	CAS LATENCY			BURST TYPE	BURST LENGTH		

12 Figs

FIG. 2

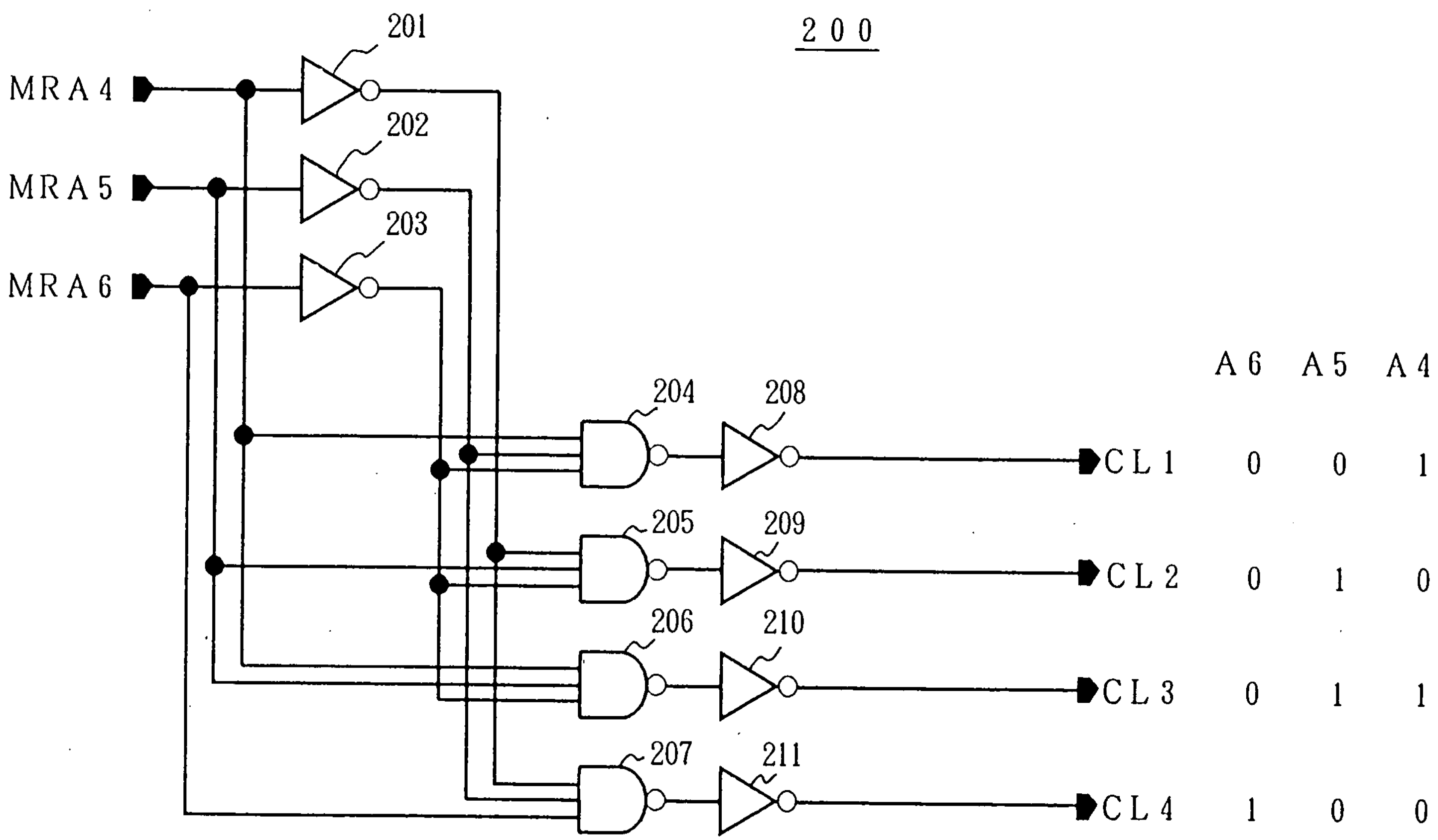

200
MRA4
MRA5
MRA6
201
202
203
204
205
206
207
208
209
210
211
CL1
CL2
CL3
CL4
A6 A5 A4
0 0 1
0 1 0
0 1 1
1 0 0

FIG. 3

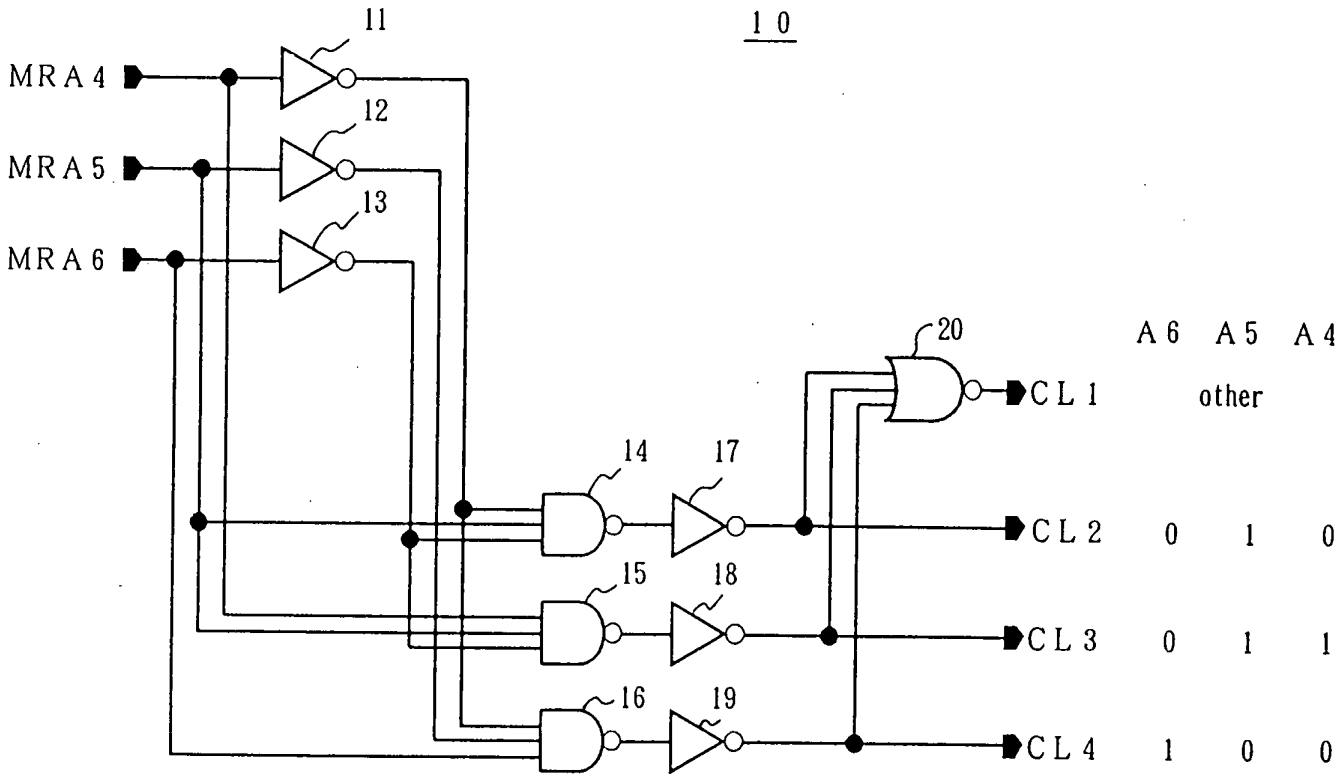

10
11
12
13
MRA4
MRA5
MRA6
14
15
16
17
18
19
20
CL1
CL2
CL3
CL4
A6 A5 A4
other
0 1 0
0 1 1
1 0 0

FIG. 4

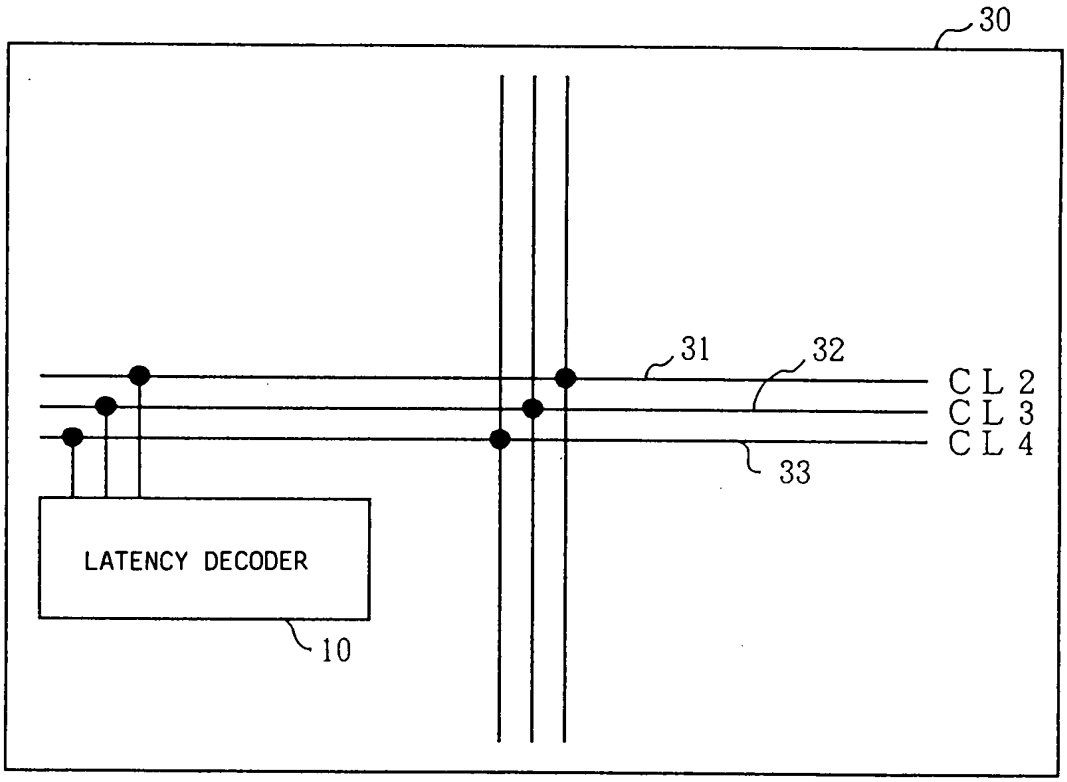


FIG. 6

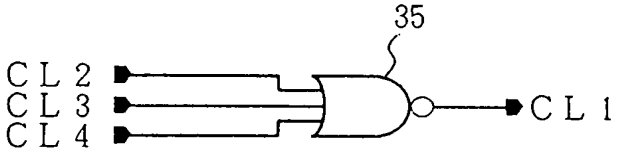


FIG. 5

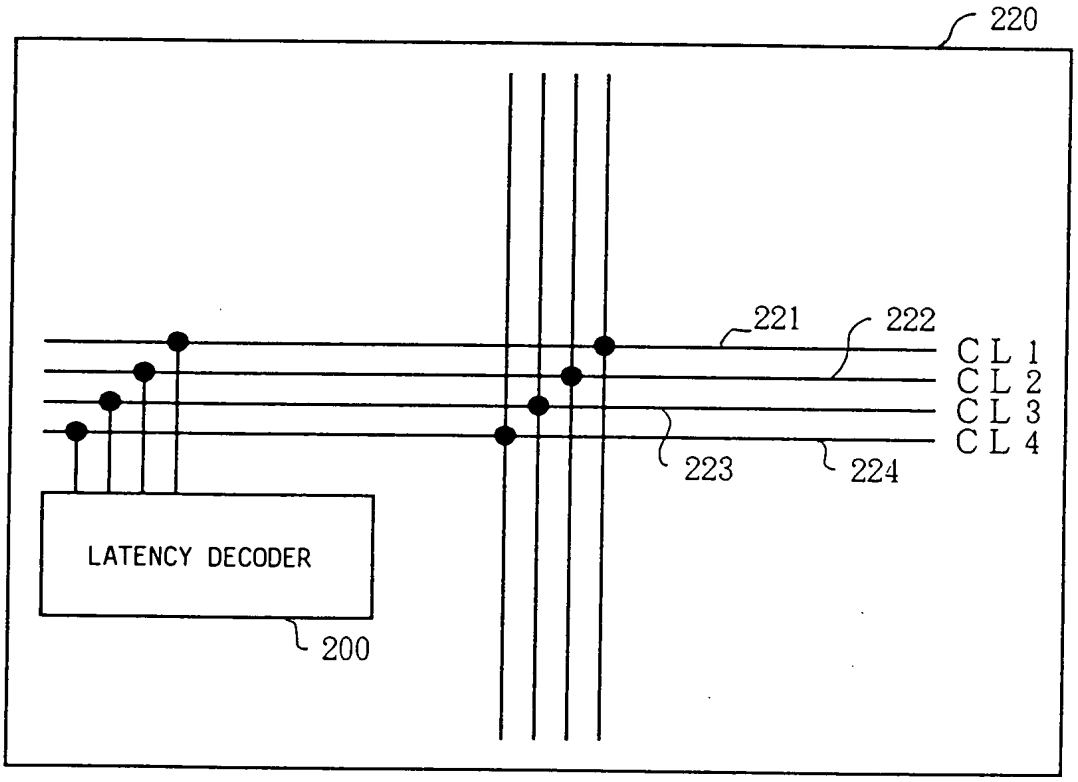


FIG.7

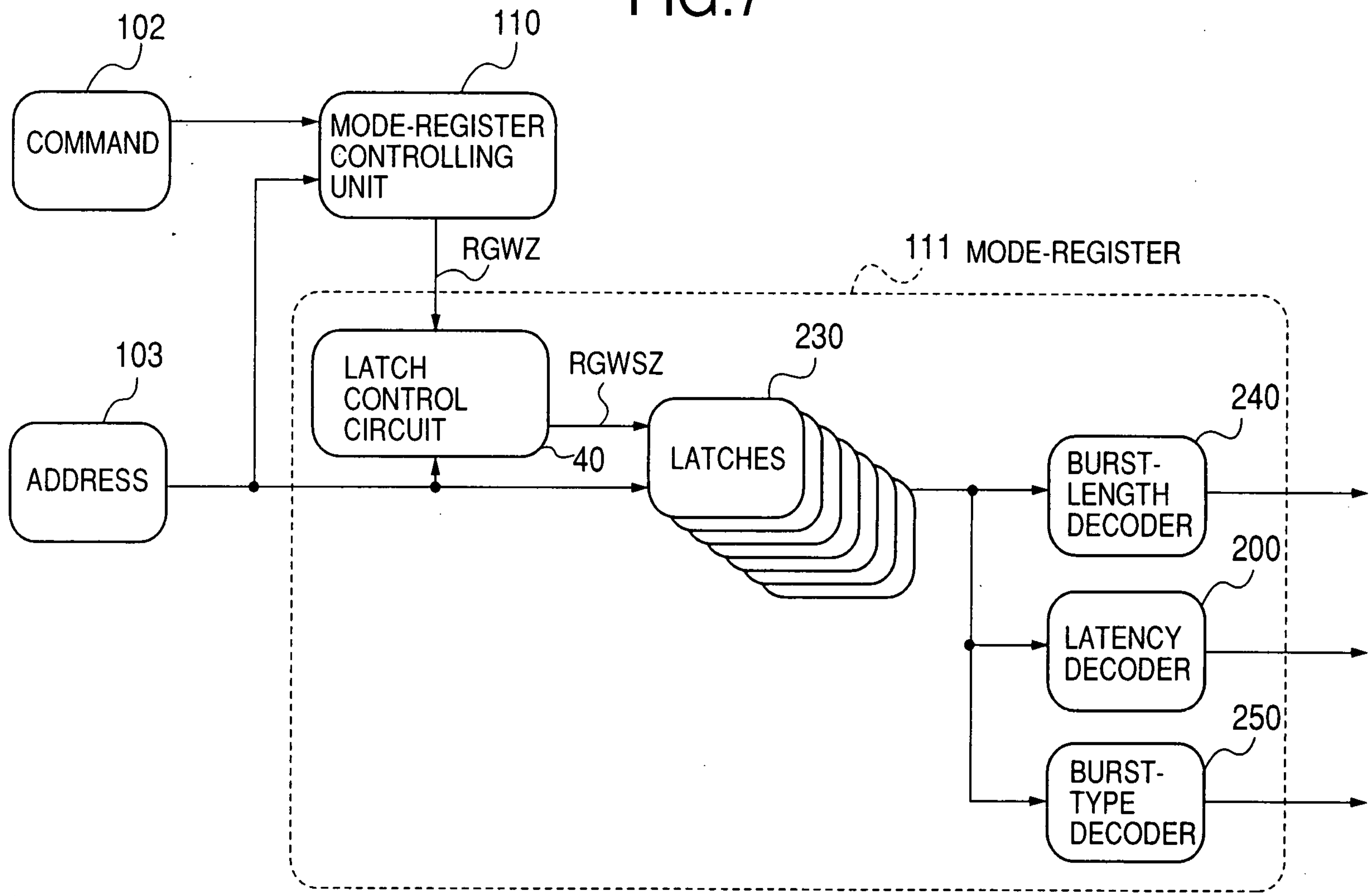


FIG. 8

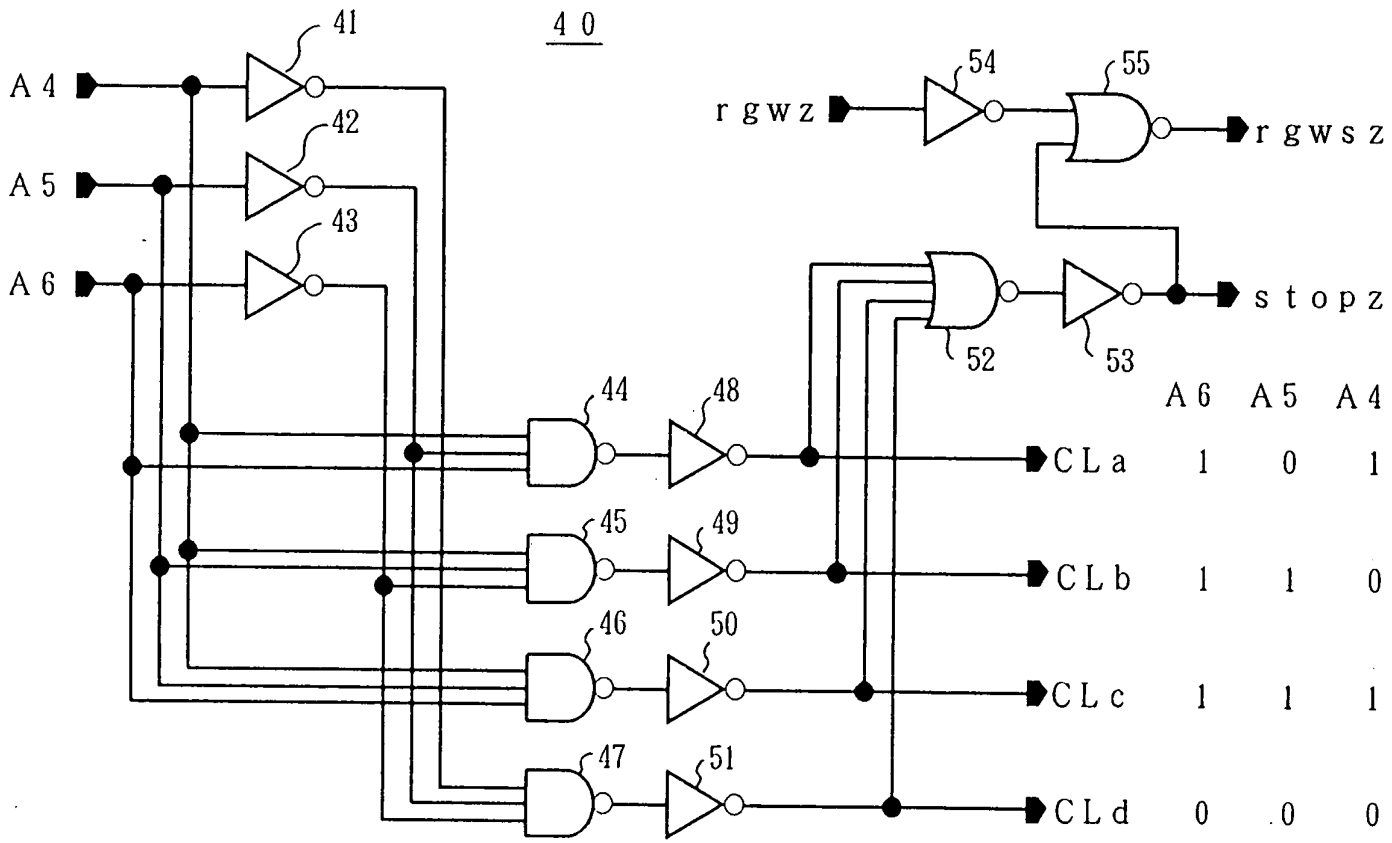
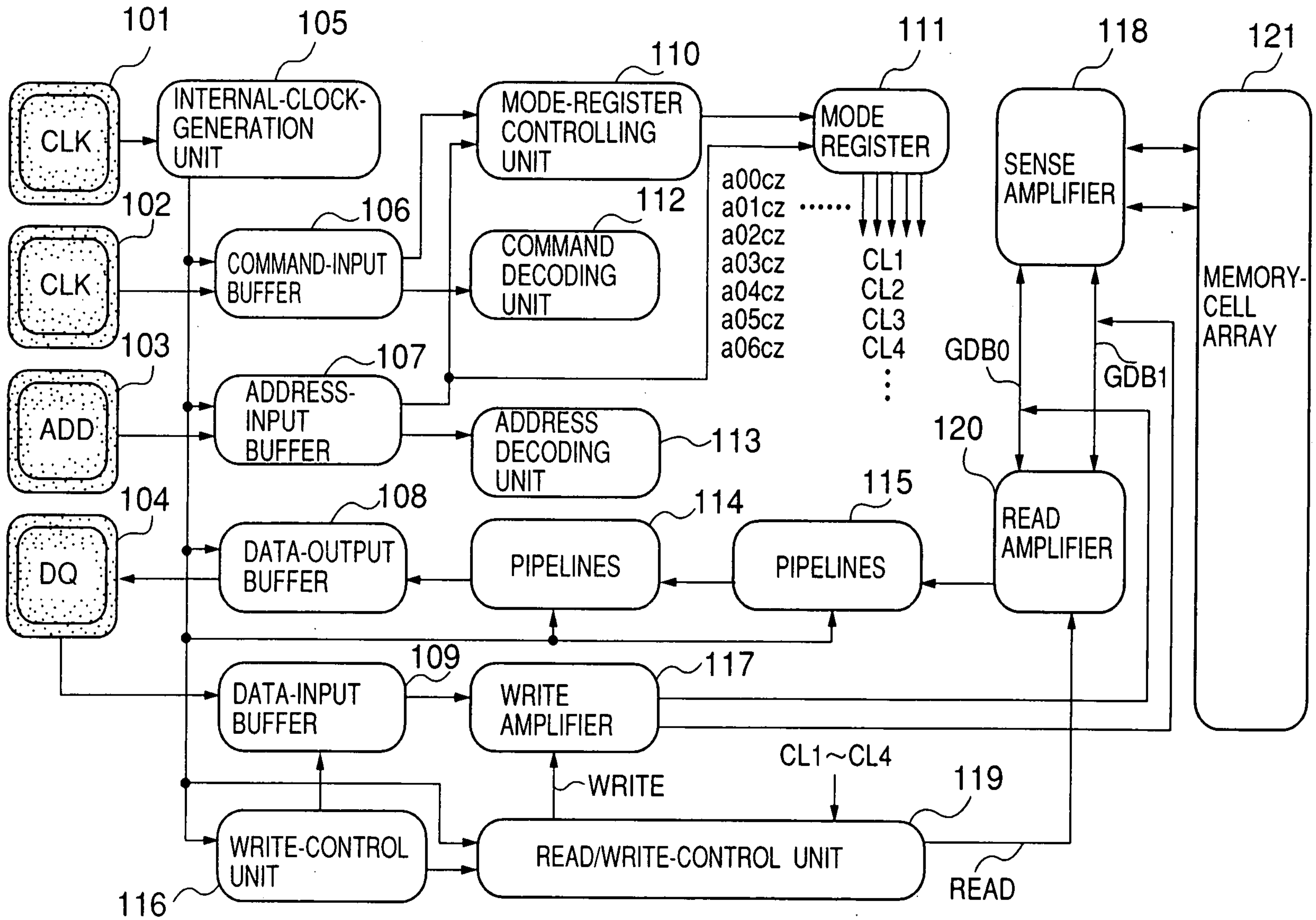

40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
A4
A5
A6
rgwz
rgwsz
stopz
CLa
CLb
CLc
CLd
A6 A5 A4
1 0 1
1 1 0
1 1 1
0 0 0

FIG.9



101
CLK
102
CLK
103
ADD
104
DQ
105
INTERNAL-CLOCK-GENERATION UNIT
106
COMMAND-INPUT BUFFER
107
ADDRESS-INPUT BUFFER
108
DATA-OUTPUT BUFFER
109
DATA-INPUT BUFFER
110
MODE-REGISTER CONTROLLING UNIT
111
MODE REGISTER
112
COMMAND DECODING UNIT
113
ADDRESS DECODING UNIT
114
PIPELINES
115
PIPELINES
116
WRITE-CONTROL UNIT
117
WRITE AMPLIFIER
118
SENSE AMPLIFIER
119
READ/WRITE-CONTROL UNIT
120
READ AMPLIFIER
121
MEMORY-CELL ARRAY
a00cz
a01cz
a02cz
a03cz
a04cz
a05cz
a06cz
CL1
CL2
CL3
CL4
GDB0
GDB1
CL1~CL4
WRITE
READ